Method for an optimum layout and noise management for charging protection devices in test chips

Disclosed is a method for an optimum layout and noise management for charging protection devices in test chips. Benefits include improved functionality and an improved test environment.

Background

Conventional test systems include protecting devices (PDs), such as transistors, substrate taps, and resistors to ground transistors. PDs are connected through a fuse that can be blown before the measurement is made. During the fuse blowing process, gate oxide stress can occur to the transistor under test. When a fuse is not completely blown, residual fuse leakage contaminates about 25% of the data population, producing inaccurate test results. Additionally, silicon surface space is required to accommodate the PDs (see Figure 1).

Fuse pads occupy ~30% of the layout space in a 24-pad test chip row. A solution is required that uses less silicon surface area and does not stress or damage the protected transistors.

General description

The disclosed method is an optimum layout and noise management for charging protection devices in test chips. The method uses one control pad to deactivate all charging PDs on the same pad row during measurement, eliminating the use of fuses and fuse pads. As a result, the method eliminates the silicon surface area requirement, prevents gate oxide degradation, and eliminates residual fuse leakage in test chips.

Advantages

The disclosed method provides advantages, including:

- Improved functionality due to providing PD control using one control pad
- Improved functionality due to reducing the silicon surface area required by using one PD control pad
- Improved test environment due to enabling consistent reproducible test results
- Improved test environment due to limiting PD leakage current

Detailed description

The disclosed method uses one control pad to deactivate all charging phase detectors in the same pad row during test measurement. For example, transistors require protection during plasma processing. The transistors are represented by boxes marked as transistor #1, #2,…, #*N*, where *N* is the total number of the transistors to be protected in a test chip pad row. Each of the transistors is protected by one PD. The same PD is used for all protected transistors. Only one pad is used to control the gate of all PDs (see Figure 2).

In complementary metal oxide semiconductor (CMOS) technology, the transistors (#1 to #*N*) to be protected can be negative or positive MOS type. For example, the PD is an NMOS with a drain connected to the gate of the transistors to be protected through a polyimide resistor, which is designated as R1. It is a current-limiting resistor, making the drain junction of the PD less forward biased during tests that require the device under test (DUT) to have a negative gate bias. The gate of the PD is connected to its source and substrate through another poly-resistor, which is designated as R2. It enables the application of a negative bias at the gate of the PD to turn off the resistor during testing. Additionally, R2 ensures that the gate of the PD is nearly at the ground (substrate) potential during plasma processing, providing sufficient subthreshold conduction current to protect the DUT. A common pad receives a negative bias, such as -0.5V. The pad is connected to the gate of each of the PDs to deactivate them during measurement (see Figure 3).

The disclosed method can be verified using experimentation. Results indicate the method minimizes layout space usage because only one extra probing pad per pad row is required. The method guarantees that no stress from a blowing fuse occurs during testing because no fuses are blown. Leakage current from the PD is limited by effectively deactivating the protecting device during measurement.

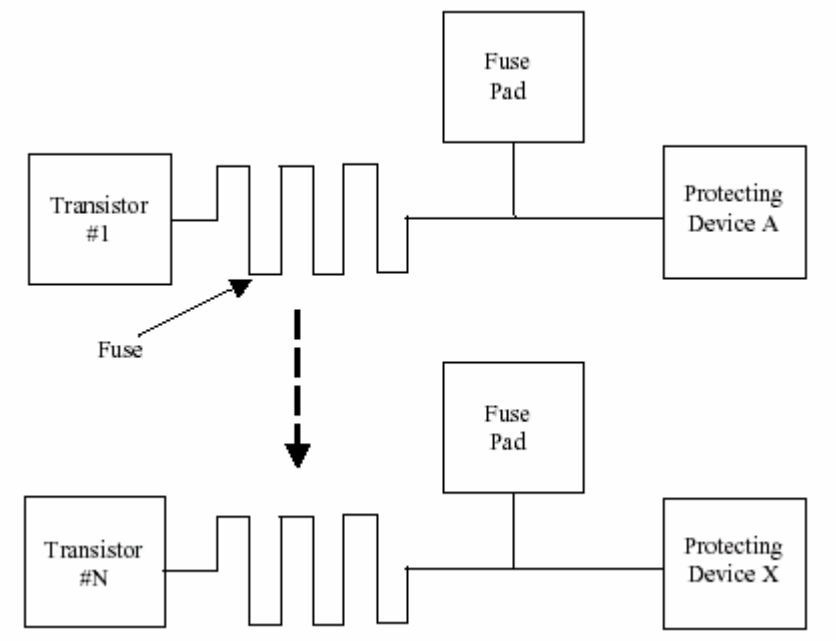

Fig. 1

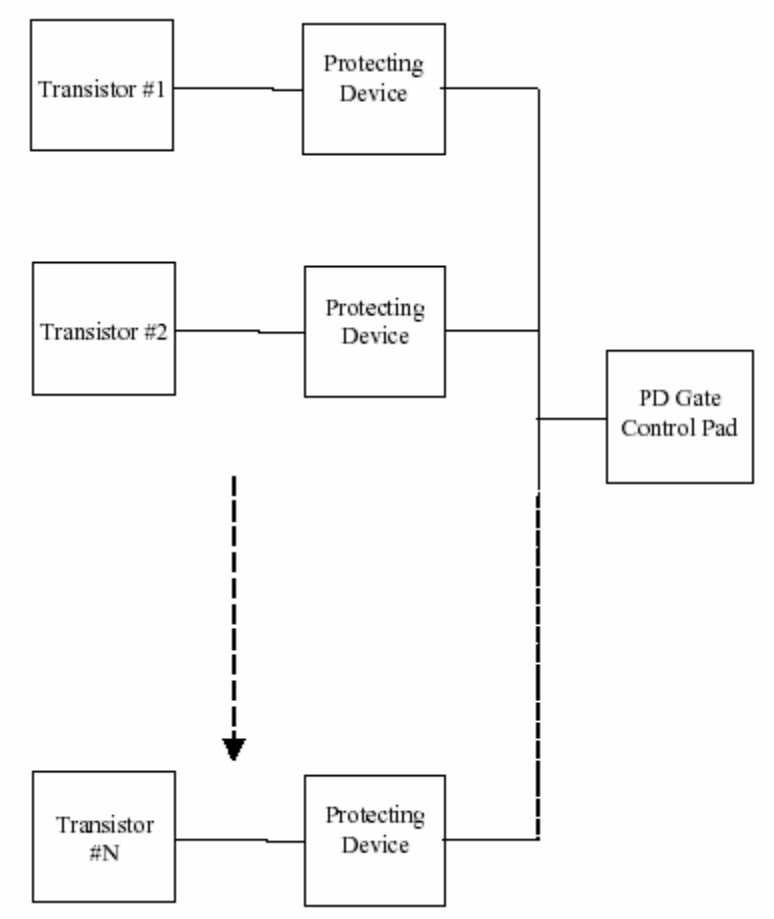
Transistor #1
Protecting Device
Transistor #2
Protecting Device
PD Gate Control Pad
Transistor #N
Protecting Device

Fig. 2

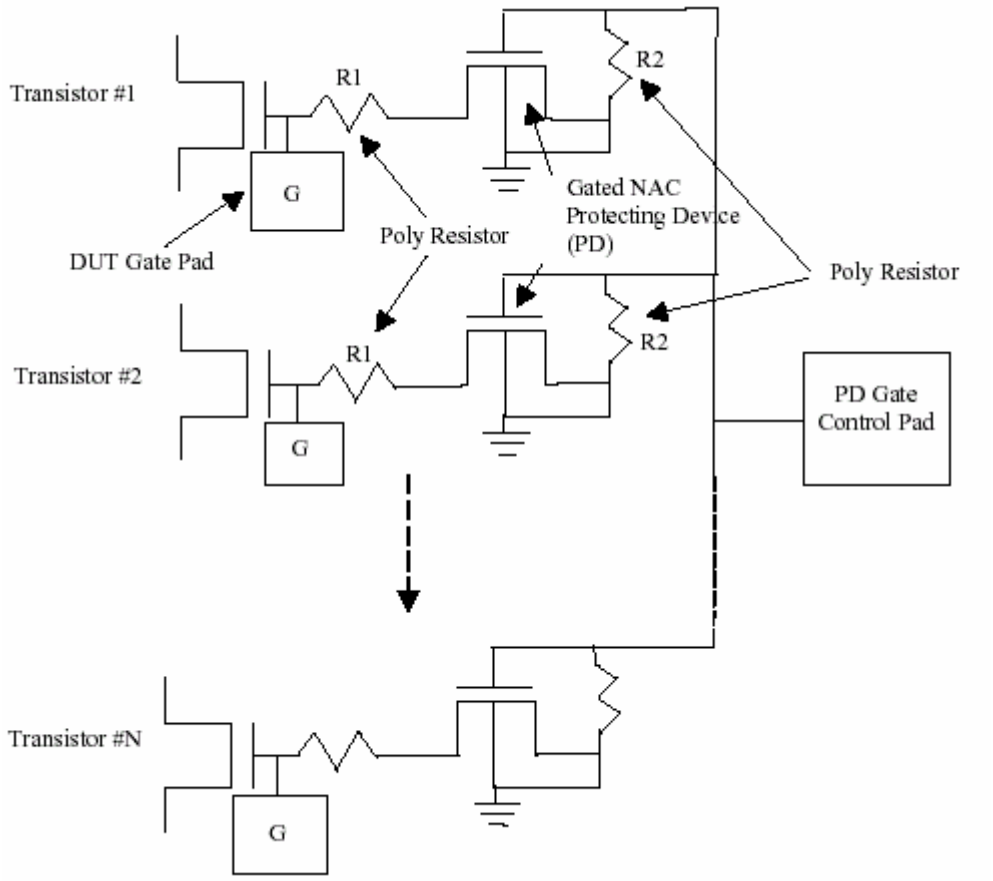

Fig. 3

Disclosed anonymously