Method for accessing internal signals on multiple-core chips during real-time debug and test

Disclosed is a method for accessing internal signals on multiple-core chips during real-time debug and test. Benefits include improved functionality, an improved debug environment, and an improved test environment.

Background

The conventional semiconductor debug and test environments do not have the capability to detect the various internal signals of multiple-core chips. A requirement exists for signal indicators, such as clock-related signals, on multiple channels for each core separately or all cores simultaneously for comparison and reference purposes.

The conventional capability is single core visibility of multiple simultaneous channels to external pins.

General description

The disclosed method accesses internal signals on multiple-core chips during real-time debug and test. The method provides information about the signals of all cores, separately or simultaneously.

The key elements of the disclosed method include:

- Externally visible package pins, on which various internal signals are routed, and test access port (TAP) accessible control registers for control and signal selection
- Driver disables for the pins and control from nonvolatile control memory (such as fuses) and/or control register bits to enable any or all cores to be idle
- Multiplexer and control from nonvolatile control memory and/or control register bits to select cores for output to each channel

Advantages

The disclosed method provides advantages, including:

- Improved functionality due to providing access to internal signals on multiple-core chips during real-time debug and test
- Improved debugging environment due to enabling detection of PLL/clock related silicon bugs on multiple-core processors
- Improved test environment due to reducing test time in proportion to a multiple of the number of cores

Detailed description

The disclosed method accesses the internal signals of multiple-core chips, using bussed external pins. Any core can be viewed independently over all channels. Alternatively, the channels can be divided among the cores to access the signals from each core. Test time involving specific signal access is halved for dual cores or multiplied in proportion to the number of cores, because all cores can be viewed simultaneously instead of sequentially. Debugging of potential PLL/clock related silicon bugs on multiple-core products is enabled, particularly when the performance, behavior, or relation between the cores must be compared or observed.

Various internal signals of any or all cores in a multiple-core chip are routed out of externally accessible package pins. The various signals are selected by setting control bits in a TAP-accessible control register. Because the cores' pins are bussed together, the ability to tristate the output driver of all but one of the cores enables one of the cores to drive unperturbed. Multiple pins (channels) are available so that multiple signals can be compared and/or referenced. All channels may be dedicated for the visibility of signals in one of the cores. Additionally, the channels may be split, some to one core, some to another, to enable the comparison/reference across the multiple cores. The external pins are not required to be dedicated for the signal output.

The disclosed method can be implemented using fuses and TAP-accessible control registers for controllability. If a particular programmable output configuration is required at product shipment, nonvolatile control memory (fuses) should be used for configuring this feature. Additionally, if the signals are required to be available at the pins during power-up sequencing debug, then non-volatile memory should be used for configuration. Otherwise, conventional control registers and/or external pins can be used.

The disclosed method can be implemented using a single channel and a dual-core processor, using four external pins. Seven control bits are used as select-bits on 4:1 multiplexers. This configuration enables the selection of up to 128 different internal signals on each of the four channels, though only a portion of them may be used. A tri-state stable output driver disables all but one of the cores to enable the remaining core to drive unperturbed. If an analog output is required, instead of a high-speed digital signal, the output can be driven directly (see Figure 1).

The disclosed method is extendable, enabling the following items to be varied:

- Number of cores
- Number of channels
- Control bits
- Selectable signals
- External pins
- Multiplexing depth
- Multiplexing breadth

A final level of multiplexing selects which of the four channels (if any) are driven out on each external pin. Not shown in the figure is the driver disable, which is in use when none of the channels are selected for a pin.

The final multiplexing is described in a table. The first row indicates that in a single-core configuration, all four channels are driven for that core. The CoreID Fuse (in column five) names the core that is driving the external pin. An “X” indicates that the core is not driving the external pin (the output driver is tri-stated). Any two channels can be selected for simultaneous viewing on both cores (see Figure 2).

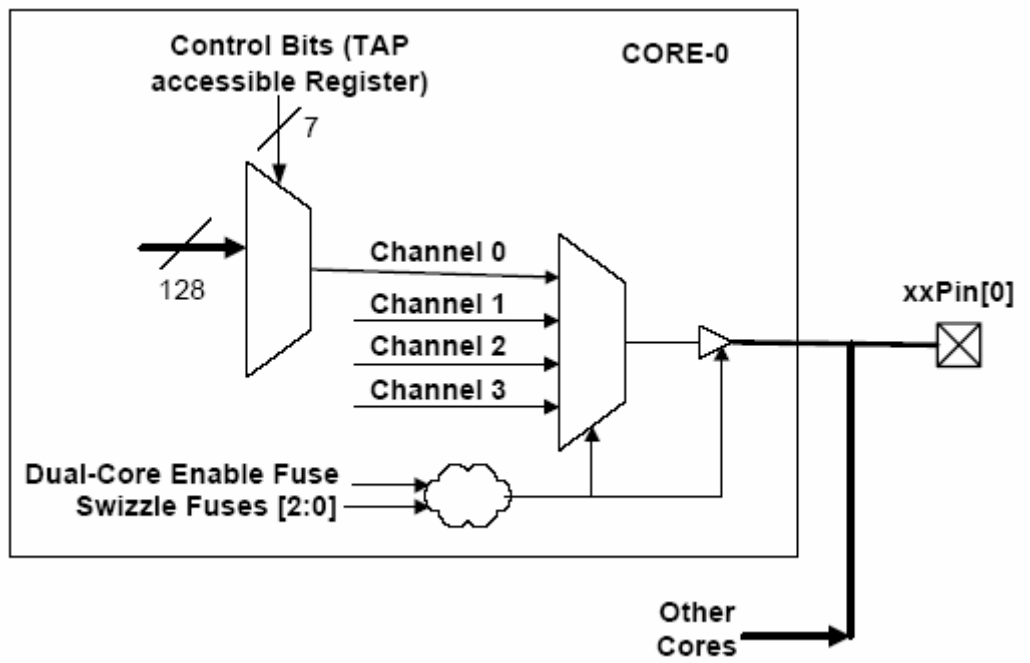

Fig. 1

Feature Control					External Pin Visibility			
Dual Core Enable? (Fuse)	Swizzle Fuse2	Swizzle Fuse1	Swizzle Fuse0	Core ID (Fuse)	xxPin[3]	xxPin[2]	xxPin[1]	xxPin[0]
0	X	X	X	X	Channel 3	Channel 2	Channel 1	Channel 0
1	0	0	0	0	Channel 3	Channel 2	X	X
1	0	0	0	1	X	X	Channel 3	Channel 2
1	0	0	1	0	Channel 3	Channel 2	Channel 1	Channel 0
1	0	0	1	1	X	X	X	X
1	0	1	0	0	Channel 3	Channel 1	X	X
1	0	1	0	1	X	X	Channel 3	Channel 1
1	0	1	1	0	Channel 3	Channel 0	X	X
1	0	1	1	1	X	X	Channel 3	Channel 0
1	1	0	0	0	Channel 2	Channel 1	X	X
1	1	0	0	1	X	X	Channel 2	Channel 1
1	1	0	1	0	Channel 2	Channel 0	X	X
1	1	0	1	1	X	X	Channel 2	Channel 0
1	1	1	0	0	Channel 1	Channel 0	X	X
1	1	1	0	1	X	X	Channel 1	Channel 0
1	1	1	1	0	X	X	X	X
1	1	1	1	1	Channel 3	Channel 2	Channel 1	Channel 0

Fig. 2

Disclosed anonymously