AN-489
Application Note

MULTIPLIER SERIES – PART I

ANALYSIS AND BASIC OPERATION OF THE MC1595

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The MC1595 monolithic linear four-quadrant multiplier is discussed. The equations for the analysis are given, along with performance that is characteristic of the device. A few basic applications are given to assist the designer in his system design.

MOTOROLA Semiconductor Products Inc.

ANALYSIS AND BASIC OPERATION OF THE MC1595

INTRODUCTION

The Motorola MC1595 four quadrant multiplier is the second basic building block now available to analog systems designers. Any control or instrumentation problem which requires the product, square, square root or ratio of two analog quantities can be easily achieved with the MC1595. Monitoring power, brake horsepower, fluid flow, solving of complex non-linear equations (using analog computer techniques), frequency doubling, phase detection, dynamic gain control, taking roots or powers, modulation circuits, navigational problems, velocity, acceleration and distance for linear or non-linear inputs, root mean square calculations, and generation of trigonometric functions are only a few of the applications for this device.

This note will be concerned with an analysis of the MC1595, the basic operating and design procedure and a few applications that will hopefully encourage the designer to consider the multiplier in his future system designs.

REVIEW OF MULTIPLICATION TECHNIQUES

There are many methods of performing analog multiplication.[1] The following partial list is offered as a brief comparison of techniques:

1. **Hall Effect** – The basic principle behind the hall effect multiplier is that the voltage across a conductor is proportional to both the current through it and the strength of the magnetic field across it.

2. **Magnetoresistance** – A magnetoresistance multiplier is basically a Wheatstone bridge made up of flux-sensitive resistors where the two variables to be multipled are the current in the coil producing the flux and the voltage across the bridge.

3. **Variable Transconductance** – A multiplier of the variable transconductance variety is based on the idea that the output of a transistor amplifier depends upon the input signal and the magnitude of the effective emitter resistance (common-emitter configuration assumed) which can be controlled by the magnitude of the emitter current. Hence, the output at the collector is proportional to the input signal times a function of the emitter current.

4. **Quarter Square** – This technique makes use of the mathematical identity $XY = 1/4\ [(X + Y)^2 - (X - Y)^2]$. Diodes are generally used to generate the square-law functions required.

5. **Pulse Height/Width** – An oscillator generates a train of rectangular pulses in which the height of the pulses is modulated by one input and the other input modulates the width. The area of the pulses is then proportional to the product of the two inputs.

6. **Triangle Averaging** – This is a variation of the quarter-square method. Instead of the square-law functions used in the quarter-square method, quadratic functions are generated by integration of clipped triangular waveforms.

7. **Logarithmic Sum** – This is the technique by which an everyday slide rule operates. XY = antilog [log X + log Y]. Log and antilog functions can be easily generated using a nonlinear element in conjunction with an operational amplifier.[2]

Of these seven methods of performing analog multiplication, the third (Variable Transconductance) is best suited to monolithic implementation. The concept of variable transconductance is used in the implementation of analog multipliers in monolithic form, the MC1595.

MULTIPLIER DISCUSSION

Multiplier circuits have been constructed using digital techniques but for reasonable accuracy the gate-count is quite high. However, the use of a linear circuit had the disadvantage of distorting at least one input due to the nonlinear processing involved. The MC1595, on the other hand, has overcome the distortion problem by preconditioning one input that cancels the nonlinear processing distortion. This preconditioning is shown in Figure 1.

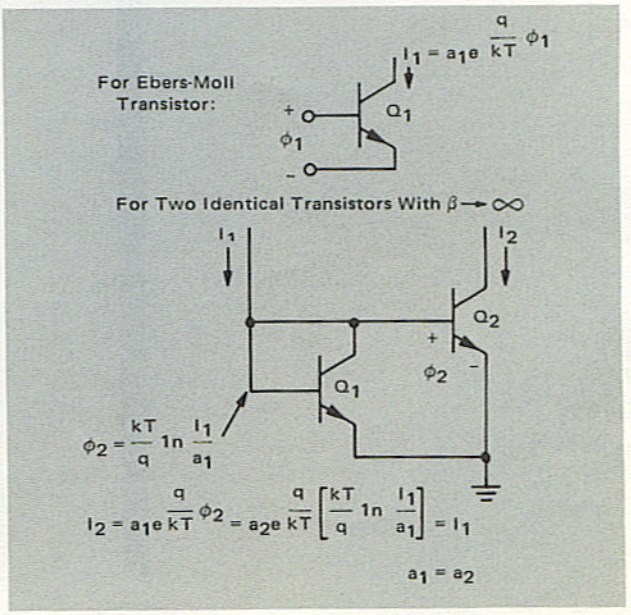


FIGURE 1 – Multiplier Preconditioning Principle

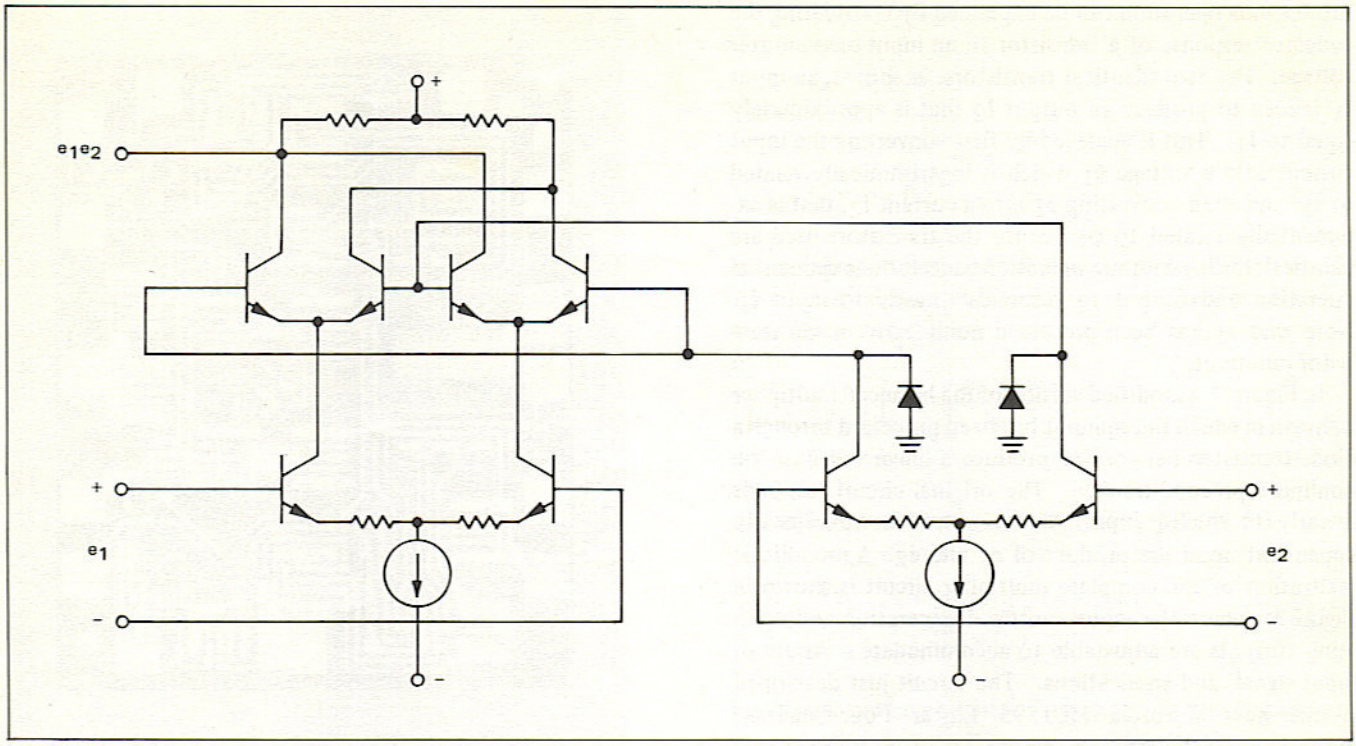


FIGURE 2 — Linear Four-Quadrant Multiplier Model

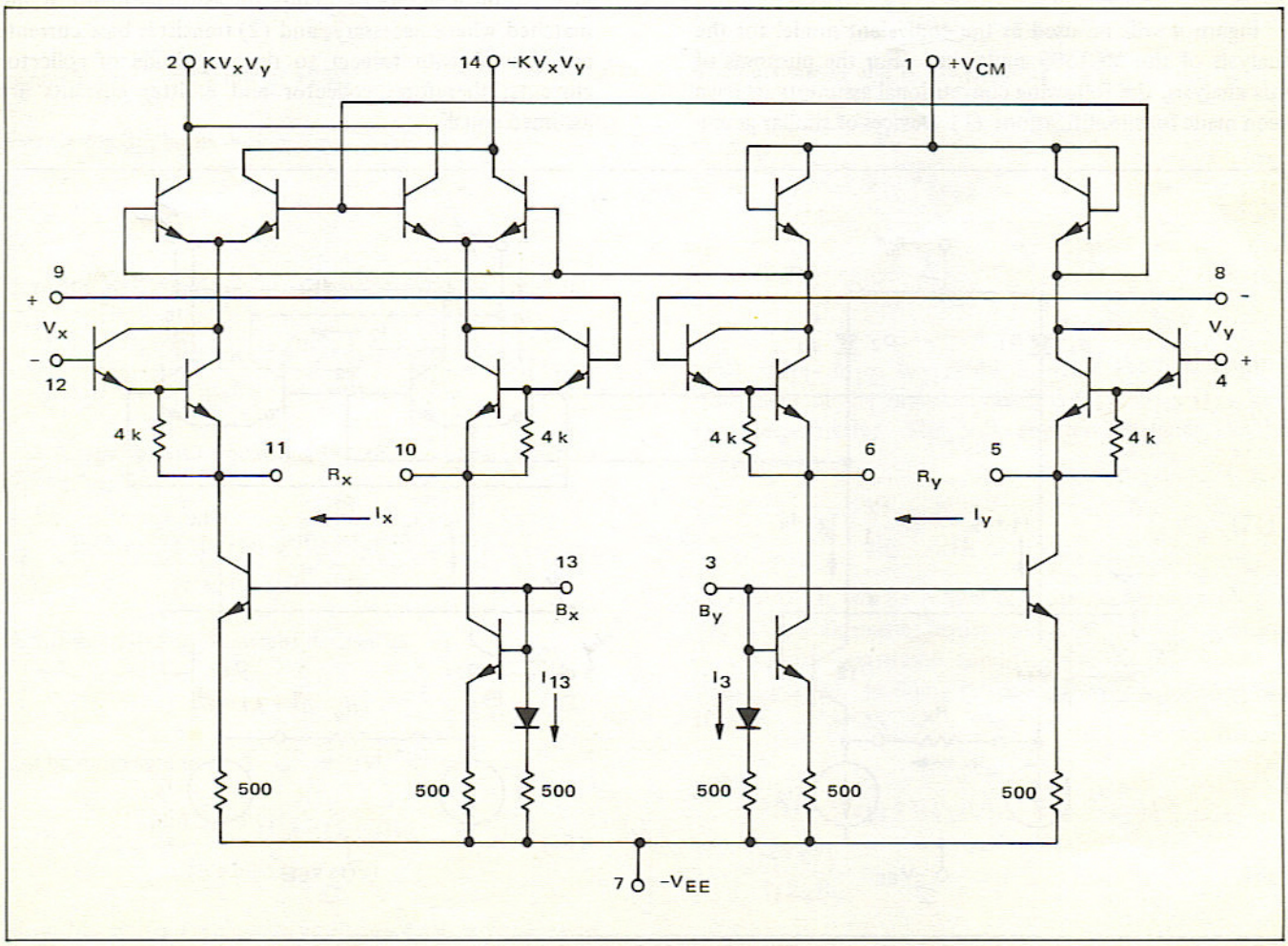


FIGURE 3a — Monolithic Realization of the MC1595 Linear Multiplier

Briefly, this operation can be explained by considering the collector response of a transistor to an input base-emitter voltage. For two identical transistors, as shown, an input I_1 is seen to produce an output I_2 that is approximately equal to I_1. This is achieved by first converting the input current into a voltage ϕ_1 which is logarithmically related to I_1, and then converting ϕ_1 into a current I_2, that is exponentially related to ϕ_1. Since the transistors used are identical, the logarithmic operation cancels the exponential operation and output I_2 responds linearly to input I_1. Note that I_1 has been processed nonlinearly in the transistor junctions.

In Figure 2, a modified version of the balanced multiplier is shown in which the e_2 input has been processed through a diode-transistor network to produce a linear response via nonlinear preconditioning. The original circuit responds linearly to the e_1 input, so the output is now linearly dependent upon the product of e_1 and e_2. A monolithic realization of the complete multiplier circuit is shown in Figure 3a, where the input emitter degeneration and operating currents are adjustable to accommodate a variety of input signals and applications. The circuit just developed is the new Motorola MC1595 Linear Four-Quadrant Multiplier. A photograph of the MC1595 die is shown in Figure 3b.

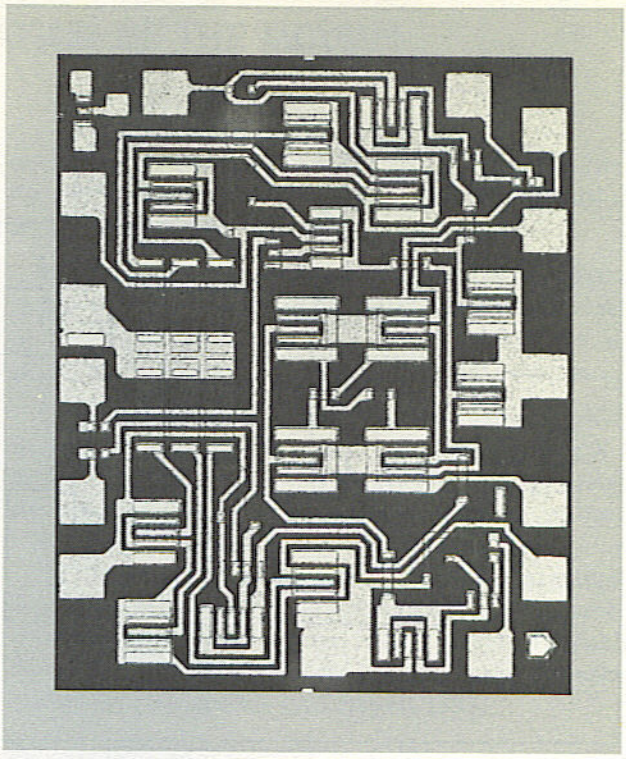


FIGURE 3b – MC1595 Die

MC1595 ANALYSIS

Figure 4 will be used as the equivalent model for the analysis of the MC1595 multiplier. For the purposes of this analysis, the following conventional assumptions have been made for simplification: (1) Devices of similar geometry within a monolithic chip are assumed identical and matched where necessary, and (2) transistor base currents are ignored with respect to the magnitude of collector currents; therefore, collector and emitter currents are assumed equal.

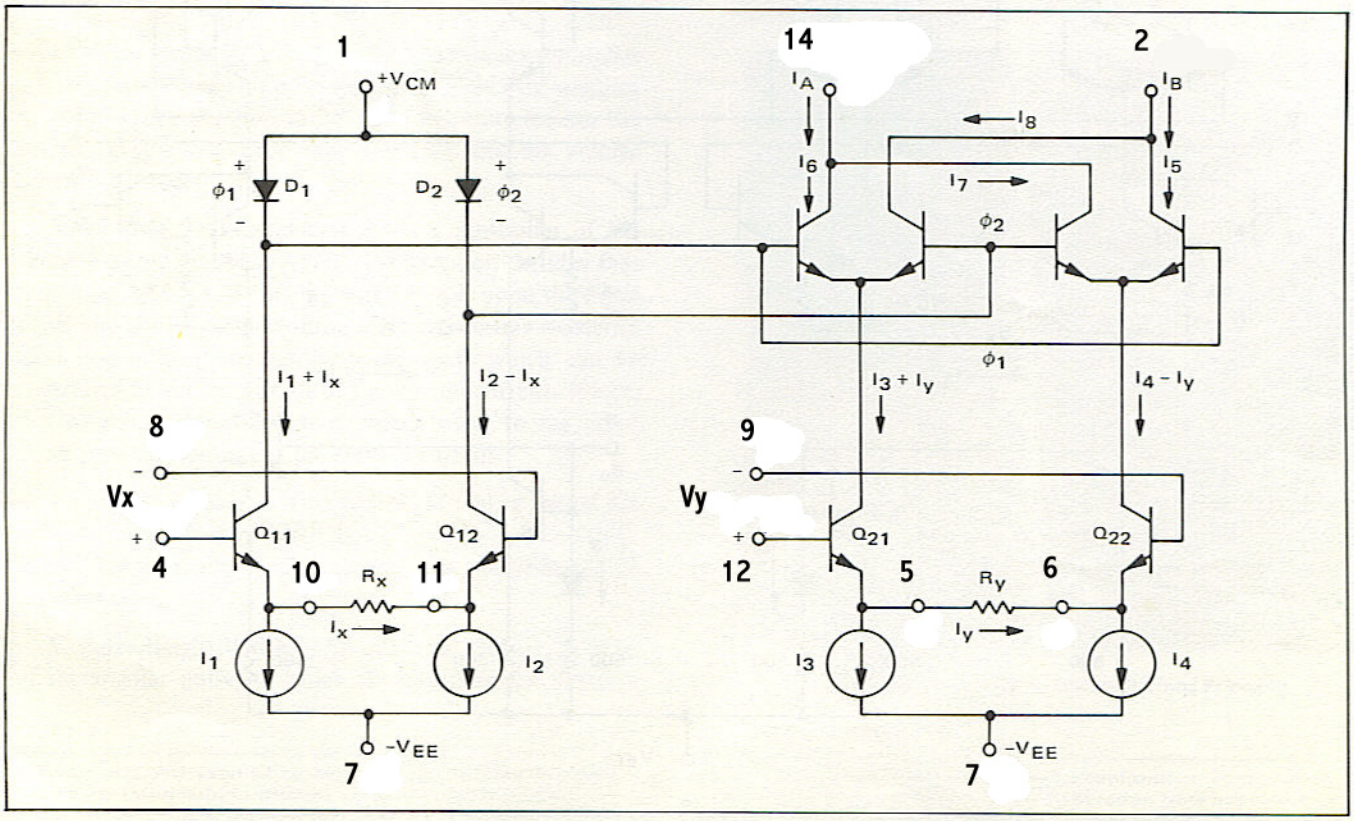


FIGURE 4 – MC1595 Equivalent Model for Analysis

From the model of Figure 4, the following equations are obtained:

$$I_3 + I_y = I_6 + I_8 \tag{1}$$

$$I_4 - I_y = I_5 + I_7 \tag{2}$$

$$I_A = I_6 + I_7 \tag{3}$$

$$I_B = I_8 + I_5 \tag{4}$$

$$I_8 = \frac{I_3 + I_y}{1 + e^{\left[\frac{\phi 1 - \phi 2}{V_T}\right]}} \tag{5}$$

$$I_5 = \frac{I_4 - I_y}{1 + e^{\left[\frac{\phi 2 - \phi 1}{V_T}\right]}} \tag{6}$$

$$I_6 = \frac{I_3 + I_y}{1 + e^{\left[\frac{\phi 2 - \phi 1}{V_T}\right]}} \tag{7}$$

$$I_7 = \frac{I_4 - I_y}{1 + e^{\left[\frac{\phi 1 - \phi 2}{V_T}\right]}} \tag{8}$$

where $V_T = \frac{kT}{q} \approx 26$ mV at +25°C.

For simplicity, let us define

$$m = \frac{\phi 1 - \phi 2}{V_T} . \tag{9}$$

Substituting (5) and (6) into (4), and solving for I_B, obtain

$$I_B = \frac{I_3(1 + e^{-m}) + I_4(1 + e^{m}) - I_y(e^{m} - e^{-m})}{(1 + e^{m})(1 + e^{-m})} \tag{10}$$

and similarily with equations (7), (8), and (3) I_A can be solved for:

$$I_A = \frac{I_3(1 + e^{m}) + I_4(1 + e^{-m}) + I_y(e^{m} - e^{-m})}{(1 + e^{m})(1 + e^{-m})} \tag{11}$$

A differential output current defined as

$$\Delta I = I_A - I_B \tag{12}$$

can be expressed as

$$\Delta I = \frac{(e^{m} - e^{-m})(I_3 - I_4 + 2I_y)}{(1 + e^{m})(1 + e^{-m})} \tag{13}$$

Now, for diodes D_1 and D_2 in Figure 4 the following can be written,

$$I_1 + I_x = a_{11}\left(e^{\frac{\phi 1}{V_T}} - 1\right) \approx a_{11}\, e^{\frac{\phi 1}{V_T}} \tag{14}$$

$$I_2 - I_x = a_{11}\left(e^{\frac{\phi 2}{V_T}} - 1\right) \approx a_1\, e^{\frac{\phi 2}{V_T}} \tag{15}$$

where the approximate equivalence is justified by assuming that the diodes are sufficiently forward biased. Further, it is observed that

$$\frac{I_1 + I_x}{I_2 - I_x} = e^{\left[\frac{\phi 1 - \phi 2}{V_T}\right]} = e^{m} \tag{16}$$

which, when substituted into equation (13), yields

$$\Delta I = \frac{(I_1 - I_2 + 2I_x)(I_3 - I_4 + 2I_y)}{(I_1 + I_2)} . \tag{17}$$

For the desired case where $I_1 = I_2$ and $I_3 = I_4$ (which can be controlled quite well on a monolithic chip),

$$\Delta I = \frac{2I_xI_y}{I_1} . \tag{18}$$

The currents I_x and I_y are given by

$$I_x = \frac{V_x}{R_x + r_{e11} + r_{e12}} \tag{19}$$

$$I_y = \frac{V_y}{R_y + r_{e21} + r_{e22}} \tag{20}$$

where r_{e11}, r_{e12}, r_{e21}, and r_{e22} are the bulk emitter resistances of the model transistors Q_{11}, Q_{12}, Q_{21}, and Q_{22} respectively. The bulk emitter resistance can be expressed as

$$r_e = \frac{kT}{qI_E} \approx \frac{26\text{ mV}}{I_E} \tag{21}$$

at +25°C. It will be shown that the maximum value for any of the bulk emitter resistances will be limited by placing a minimum constraint condition on the I_E terms in Equation (21). In doing so, the following approximation is seen:

$$\Delta I = \frac{2V_xV_y}{I_1(R_x + r_{e11} + r_{e12})(R_y + r_{e21} + r_{e22})} \approx \frac{2V_xV_y}{I_1R_xR_y}, \tag{22}$$

and if I_A and I_B from Equation (12) are dropped across a

load resistor (R_L), a differential output voltage approximation would be

$$\Delta V_o = \Delta I R_L$$

$$\approx \frac{2R_L V_x V_y}{I_1 R_x R_y} \qquad (23)$$

which illustrates the four-quadrant capability of the MC1595, giving sign and magnitude information linearly with respect to each input.

If the approximations of Equations (22) and (23) are to be valid, the bulk emitter resistances must be kept small to minimize the error introduced by the currents I_x and I_y. For example, with I_x and I_y in the direction shown in Figure 4 and $I_1 = I_2$, $I_3 = I_4$ as discussed previously, then the bulk resistances seen in the model circuit are

$$r_{e11} \approx \frac{V_T}{I_1 + I_x},$$

$$r_{e12} \approx \frac{V_T}{I_1 - I_x},$$

$$r_{e21} \approx \frac{V_T}{I_3 + I_y},$$

$$r_{e22} \approx \frac{V_T}{I_3 - I_y}, \qquad (24)$$

where, as before, $V_T \approx 26$ mV at +25°C. The two "problem" resistances are r_{e12} and r_{e22}. r_{e12} will become very large as $(I_1 - I_x)$ approaches zero. That is, if $I_1 = I_x$, then transistor Q_{12} is not conducting and the r_{e12} appears to be quite large. Considerable nonlinearity and distortion will result if the emitter currents are ever allowed to become too small. As a working constraint, the emitter currents will never be lower than one-third the value fixed in the current sources I_1 (= I_2) or I_3 (= I_4)

From Figure 3, values of the current sources are set by applying a bias voltage to pins 3($I_1 = I_2$) and 13($I_3 = I_4$). Referring once again to Figure 3, and recalling that we have assumed that base currents can be ignored in calculations, then the current flowing into pin 3 is equal to the value of each of the current sources designated I_1 and I_2 in Figure 4, and similarily the current flowing into pin 13 is equal to the value of each of I_3 and I_4 in Figure 4. To avoid any further confusion in notation, we will designate the current into pin 3 as I_3 and the current into pin 13 as I_{13} (as illustrated in Figure 3).

By using the emitter current constraints (see next section, "Using the Multiplier"), the bulk emitter resistances can be less than 1% of the emitter degeneration resistors (R_x and R_y), and hence can be ignored. Therefore, the differential output voltage can be expressed as

$$V_o = KV_xV_y, \qquad (25)$$

where

$$K = \frac{2R_L}{I_3 R_x R_y} = .1 \qquad (26)$$

USING THE MULTIPLIER

From the previous circuit analysis of the MC1595, the circuit of Figure 5 illustrates the basic configuration for using the multiplier.

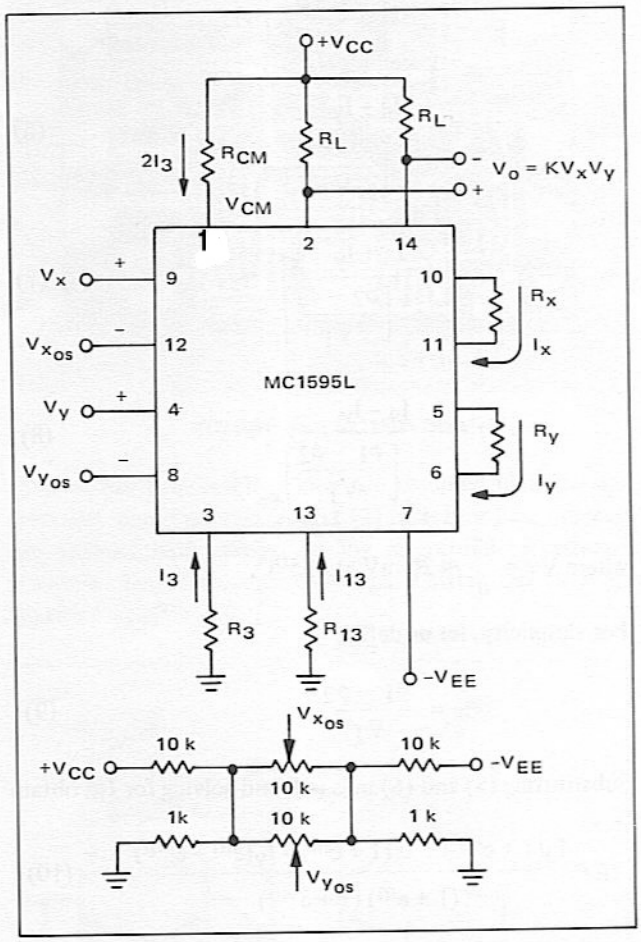


FIGURE 5 – Basic Multiplier Configuration

To demonstrate the thought process one would go through in the initial design phase, consider the following example which is widely used in multiplier applications.

Example:

Input Voltage Ranges:

$-10\text{ V} \leqslant V_X \leqslant +10\text{ V}$

$-10\text{ V} \leqslant V_y \leqslant +10\text{ V}$

Output Dynamic Swing: ±10 V

$$K = \frac{1}{10}$$

A good place to begin is the current sources since most other decisions will depend on their value.

The value of the current sources I_3 and I_{13} can be determined by applying a known potential to pins 3 and 13 respectively. One should select a value of current that will keep the chip power dissipation to an acceptable value and still maintain operation in a good exponential portion of the diode curve. A value of 0.5 mA to 2.0 mA is seen to be feasible, and a value of 1.0 mA is used to illustrate the operation of the device in this example. The value of the current sources can be fixed once the value of the negative supply has been chosen. A negative supply of -15 volts has been selected for this mode of operation which will allow a -10 V input capability and insure linear operation in the current source transistor, and stay within the 30 volt MAXIMUM RATING between any input pin and the negative supply pin (as specified in the data sheet). With $-V_{EE}$ = -15 V, the current sources are each set to 1.0 mA by putting a resistor from pin 3 to ground and from pin 13 to ground as

$$(R + 500\Omega)\,(1\text{ mA}) = (15 - 0.7)\text{V}$$
$$R = 13.8\text{ k}\Omega \qquad (27)$$

where the forward voltage of a silicon diode is assumed to be 0.7 volts. Since this is not a critical adjustment, a convenient value of 13.7 kΩ, 1/4 W composition is used.

Recalling the emitter current constraints, from which we were able to ignore the bulk emitter resistance terms, the following is seen for the emitter resistors R_X and R_Y:

$$R_X = \frac{V_{x(max)}}{I_{x(max)}} \qquad (28)$$

$$= \frac{V_{x(max)}}{2/3\,(I_{13})} \qquad (29)$$

$$= \frac{+10\text{ V}}{2/3\,(1.0\text{ mA})}$$

$$= 15\text{ k}\Omega$$

and

$$R_y = \frac{V_{y(max)}}{I_{y(max)}} \qquad (30)$$

$$= \frac{V_{y(max)}}{2/3\,(I_3)} \qquad (31)$$

$$= \frac{+10\text{ V}}{2/3\,(1.0\text{ mA})}$$

$$= 15\text{ k}\Omega.$$

R_X and R_Y are equal in this example because the maximum voltage at both inputs are equal, which is not necessarily so in all applications.

From Equation (26) the value of the load resistors are each found to be

$$R_L = \frac{KI_3R_xR_y}{2}$$

$$= \frac{(10^{-1})(10^{-3})(15 \times 10^3)(15 \times 10^3)}{2}$$

$$= 11.25\text{ k}\Omega \qquad (32)$$

and if I_3 is varied slightly, a standard value 11 kΩ resistor can be used. To vary I_3, R_3 is a 10 k resistor in series with a 5 k pot. At this point, everything necessary for operation of the device has been specified except the common-mode resistor (R_{CM}) at pin 1 and the positive supply ($+V_{CC}$).

With a +10 V input at V_y, the voltage at the collectors of the V_y-input differential amplifier should be about 13 V to insure linear operation; hence, the common-mode voltage at pin 1 must be about +13.7 V. The +13 V collector potential appears at the bases of the cross-coupled differential pair where the minimum collector potential, again to insure linear operation, should be about +16 V. With a minimum of about 16 volts and a 10 volt swing, the quiescent collector potential is about 21 volts. In this quiescent condition the current source value (1 mA) is seen in each load resistor (11 kΩ); therefore, a positive supply of 32 volts is required. Using $+V_{CC}$ = +32 V, the desired voltage at pin 1 is obtained through a common-mode resistor, R_{CM} as

$$R_{CM} = \frac{(32 - 13.7)\text{V}}{2\text{ mA}}$$

$$= 9.15\text{ k}\Omega. \qquad (33)$$

Since the collector potential is not critical, a value of 9.1 kΩ, is acceptable.

To summarize the operating configuration:

$+V_{CC}$ = +32 V
$-V_{EE}$ = -15 V
R_{13} = 13.7 kΩ
R_3 = 10 kΩ + 5 kΩ pot (Gain Adjust)
$R_X = R_Y$ = 15 kΩ
R_L = 11 kΩ
R_{CM} = 9.1 kΩ

which is illustrated in Figure 6.

One final item that needs to be mentioned is that each input will exhibit some input offset voltage, which can be nulled as shown in Figure 6. Also, the differential output will exhibit some offset, which can be nulled as shown.

A brief set-up procedure is as follows:

SET-UP PROCEDURE (FIGURE 6)

1. Set $V_X = V_y = 0$ and adjust differential output offset to zero.
2. Set V_X = 5.0 V, V_y = 0.0 V and adjust V_y-offset until output is zero.
3. Set V_y = 5.0 V, V_X = 0.0 V and adjust V_X-offset until output is zero.
4. Repeat Step 1.
5. Set $V_X = V_y$ = +5.000 V and adjust gain control until output is +2.500 V.
6. Set $V_X = V_y$ = -5.000 V. If output error is appreciable, repeat steps 1 through 5.

When the multiplier is operated in a dc mode, the dc output at pins 2 and 14 will ride a large common-mode voltage (≈ +22 volts in this example). Some common-mode level translating circuits will be shown in the following section; however, the present circuit (Figure 6) can be operated in an ac mode where the output can be very effectively ac-coupled.

The output response exhibits a single pole characteristic, due to R_L and stray (or load) capacitance. In an operating condition where R_L = 5.6 kΩ the bandwidth capability of the multiplier is observed and illustrated in Figure 7. Here, one input is a constant 1-volt dc and the other is 1 V(rms). The output is 0.1 V(rms) out to 1 MHz, is 3 dB down at 4.5 MHz, and 10 dB at about 14 MHz. The frequency response curve exhibits a single pole characteristic, with the pole located about 4.5 MHz. At this frequency, their exists 45° of phase shift. Hence, the single-ended output can be expressed as

$$V_O = V_X V_y \text{Cos}\theta, \qquad (34)$$

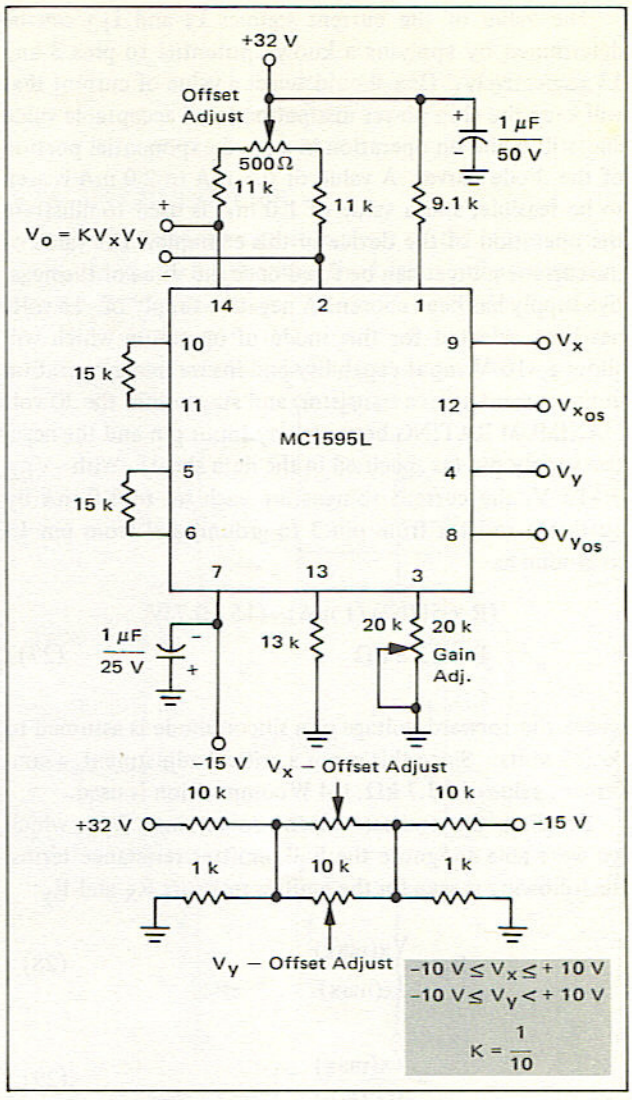


FIGURE 6 – Basic Multiply Circuit

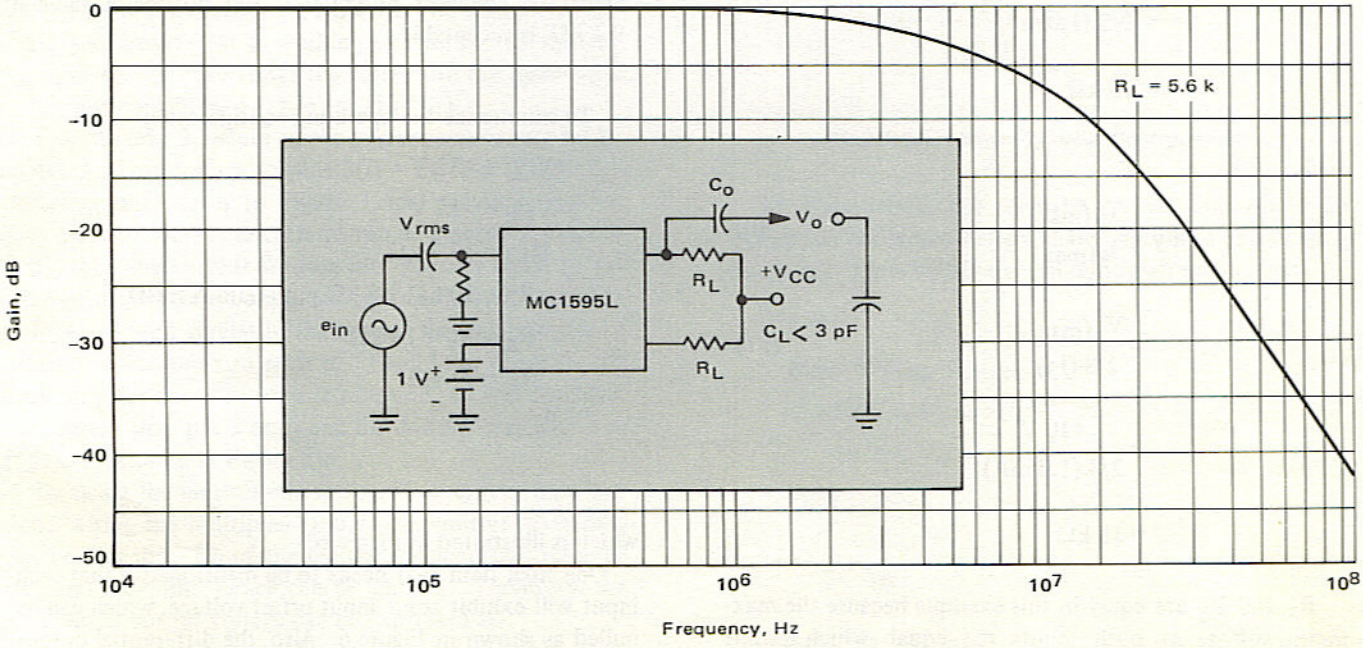


FIGURE 7 – Multiplier Bandwidth

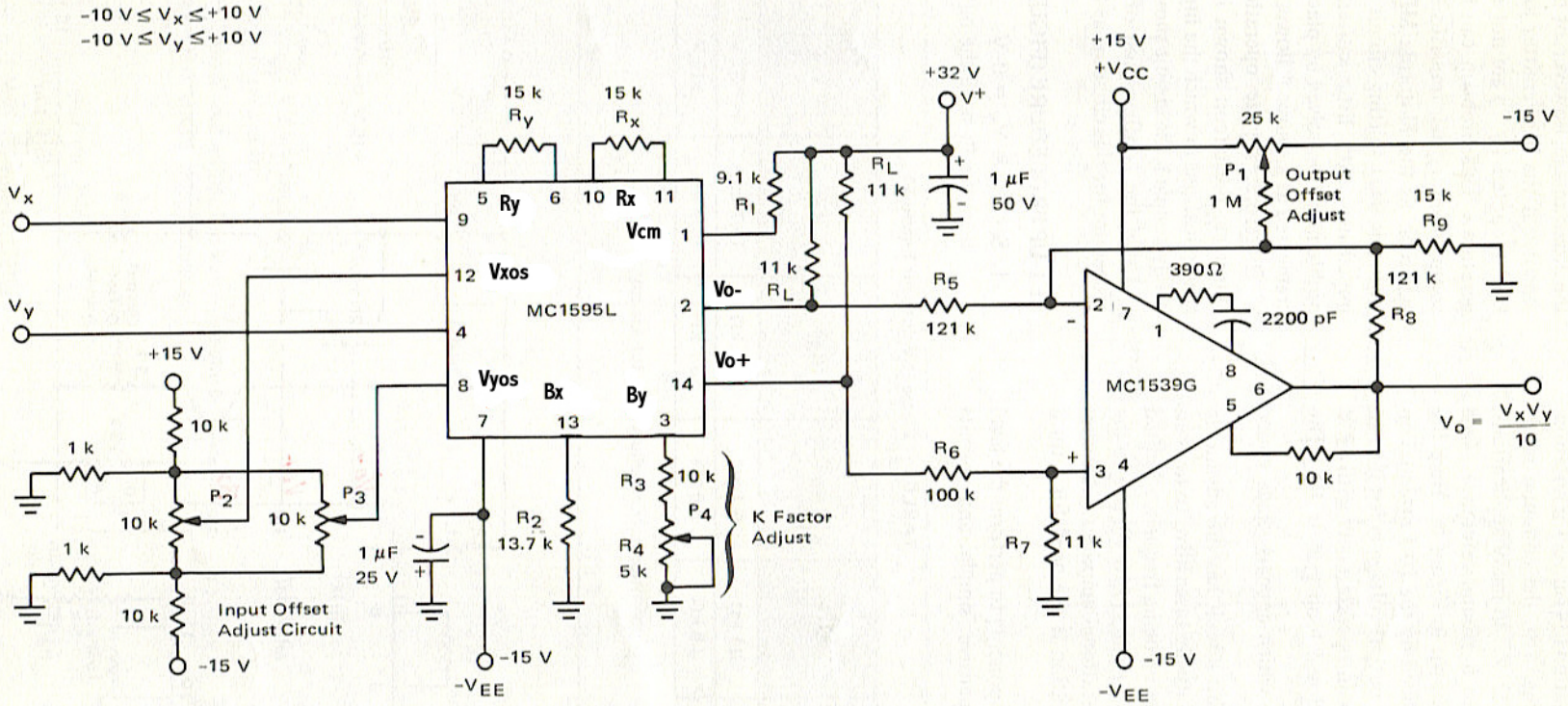


FIGURE 8 — Multiply with Op Amp Level Shift

where in Figure 7, V_X = +1.0 Vdc, V_Y = 1.414 Cosωt, and θ is the relative phase shift observed due to roll-off. A 3° roll-off will cause the output to fall off by about 0.15%, which ideally occurs at each output, as can be visualized by representing Equation (34) in vector notation.

In the configuration of Figure 6, the common mode output is seen to be about +22 V. In many applications, it is desirable to level shift to a ground reference. One method of obtaining this is shown in Figure 8. Here the common-mode voltage is reduced by the 10-1 attenuation networks and the differential output voltage is fed into an operational amplifier, which can operate easily with +2 V common-mode, and whose closed loop gain is 10. The resulting output is still $\frac{V_X V_Y}{10}$ which appears single ended about a ground reference. This circuit has the advantage of being rather simple and relatively insensitive to temperature. It has the disadvantage of being frequency limited to about 50 kHz for large signal swings (±10 V), due to the slew rate of the MC1539 operational amplifier. Another disadvantage of this configuration is the need for a third power supply.

Figure 9 uses discrete components to perform the level shifting making it very inexpensive, simple, and permits operation at higher frequencies (limited by the 7.5 kΩ resistor and stray capacitance associated with the output). The circuit of Figure 9 also has the added advantage of operating entirely from ±15 V supplies. This circuit has the disadvantage, however, of being somewhat temperature sensitive if the base emitter junctions of the NPN and the PNP (denoted by *) are not matched to track with temperature. This problem can be greatly reduced by using complementary pair transistors mounted in the same package such as the Motorola MD6100. A second problem with this level shifting circuit is that it has a high output impedance with little current drive capabilities. The problem can be solved by placing an operational amplifier connected as a source follower as shown in Figure 10.

Therefore, for dc operation over wide temperature extremes, the circuit shown in Figure 8 is preferred; for ac applications in which the input and output can be capacitively coupled, the circuit shown in Figure 9 is preferred.

Using the configuration of Figure 8, a general set-up procedure for this circuit is as follows:

SET-UP PROCEDURE (FIGURE 8)

1. Set $V_X = V_Y = 0$ V. Adjust output offset potentiometer P_1 until the output reads zero volts.

TABLE I — Element Values for Figure 11

V_X|max V_Y|max V_{out}|max	R_X R_Y	R_L	R_1	R_3*	R_{13}	V_{CC}	V_7	V_{CM}
±10 V	15 kΩ	11 kΩ	9.1 kΩ	13.7 kΩ	13.7 kΩ	+32 V	-15 V	+21 V
±5 V	8.2 kΩ	3.3 kΩ	3.9 kΩ	13.7 kΩ	13.7 kΩ	+15 V	-15 V	11.7 V

*Value given for R_3 is approximate — use potentiometer to adjust K factor exactly.

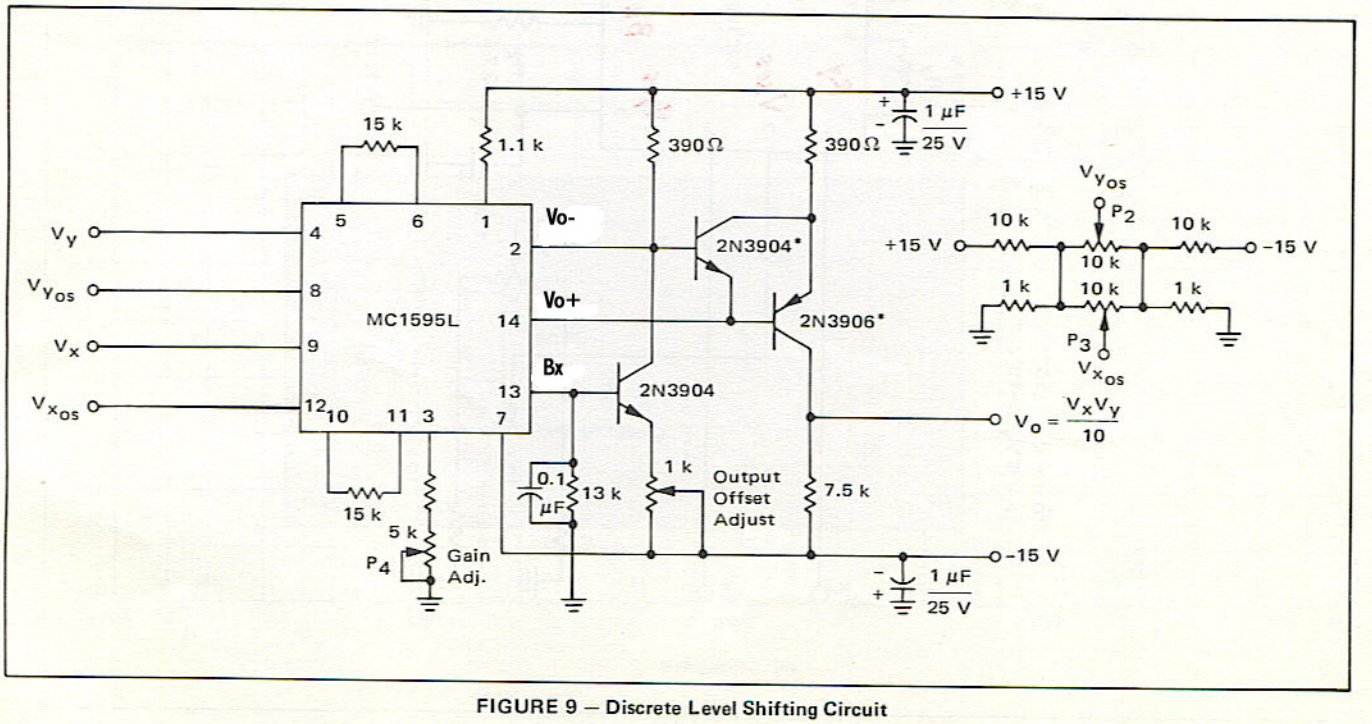


FIGURE 9 — Discrete Level Shifting Circuit

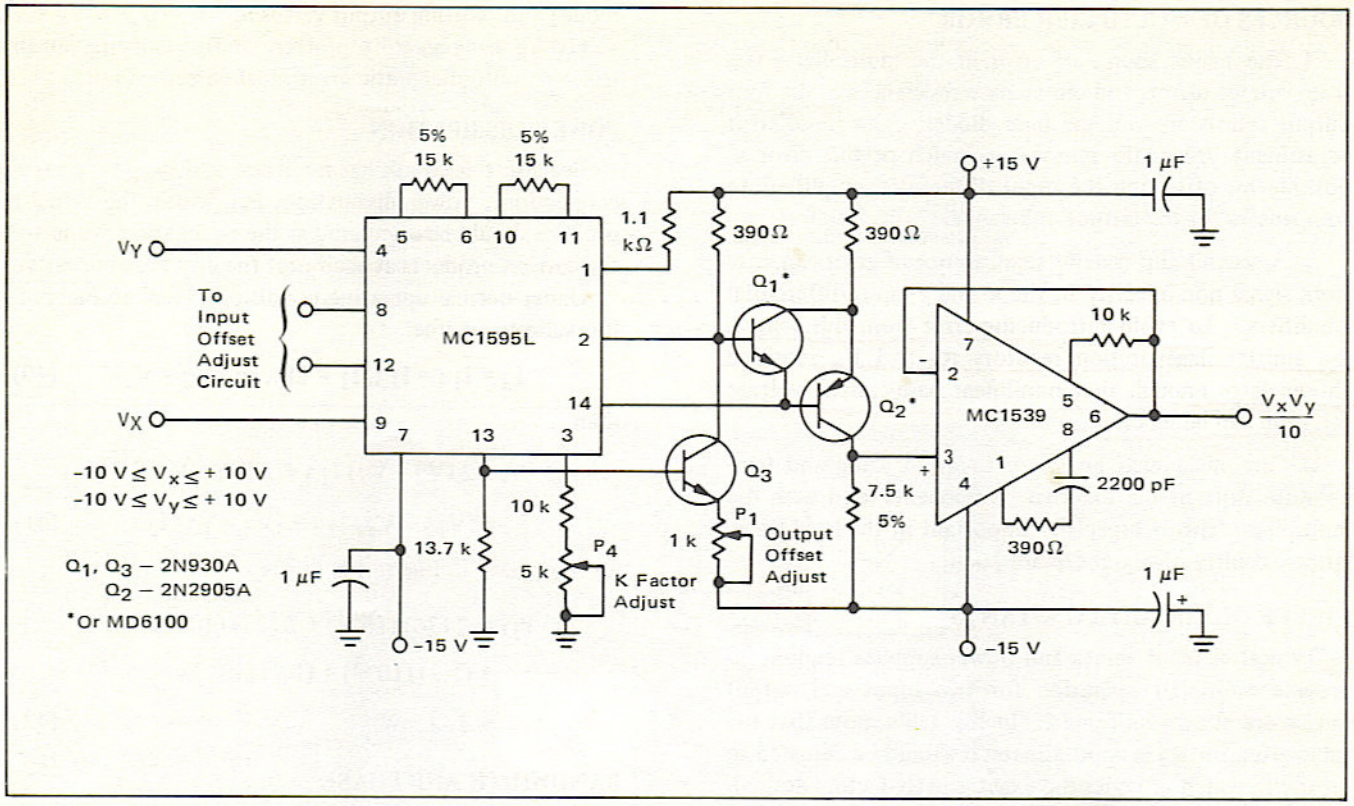


FIGURE 10 – Multiply with Discrete Level Shift

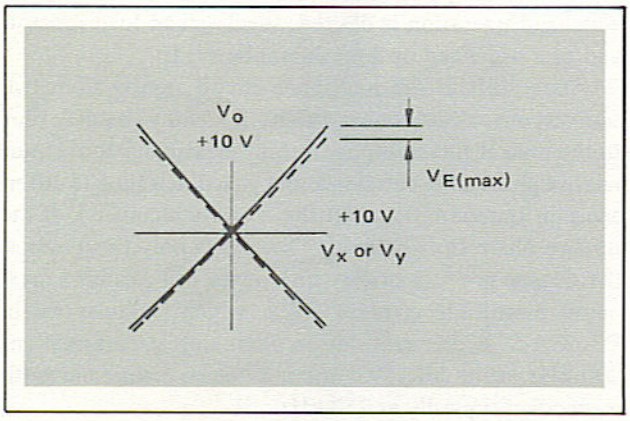


FIGURE 11 –

2. Set V_X = 5.000 V, V_y = 0.000 V and adjust potentiometer P_3 until output reads zero volts. **(Vxos)**
3. Set V_y = 5.000 V, V_X = 0.000 V and adjust the voltage at pin 9 (Potentiometer P_2) until output reads zero volts. **(Vyos)**
4. Repeat Step 1.
5. Set $V_X = V_y$ = 5.000 V and adjust the gain potentiometer (P_4) until output reads -2.500 V.
6. Set $V_X = V_y$ = -5.000 V and note the output. The output should again be -2.500 V. If the error is appreciable (greater than 1 or 2 percent), repeat steps 1 through 6.

To summarize the set-up process, the following equations are seen (Ref - Figure 5):

$$I_3 = \frac{-0.7\ V - (-V_{EE})}{R_3 + 500\ \Omega} \tag{35}$$

$$I_{13} = \frac{-0.7\ V - (-V_{EE})}{R_{13} + 500\ \Omega} \tag{36}$$

$$R_{CM} = \frac{+V_{CC} - V_{CM(pin\ 1)}}{2I_3}. \tag{37}$$

For the constraint (r_e is neglected):

$$I_{x(max)} \leqslant (2/3)\, I_{13}$$

$$I_{y(max)} \leqslant (2/3)\, I_3$$

$$R_X = \frac{V_{x(max)}}{I_{x(max)}} = \frac{V_{x(max)}}{(2/3)\, I_{13}} \tag{38}$$

$$R_y = \frac{V_{y(max)}}{I_{y(max)}} = \frac{V_{y(max)}}{(2/3)\, I_3}. \tag{39}$$

$-V_{EE}$ is selected by knowing V_X and V_y maximum negative values.

$+V_{CC}$ is selected knowing V_X, V_y, R_L, and I_3, I_{13}.

SOURCES OF MULTIPLIER ERROR

A. The major source of error in the multiplier arises from voltage offsets and ohmic base resistances in the four output transistors and the base diodes. The static error adjustment procedure removes as much of this error as possible by offsetting the input differential amplifiers to compensate for the output unbalance.

B. A second and usually small source of error can arise from signal non-linearity in the x- and y-input differential amplifiers. To avoid introducing error from this source, the emitter degeneration resistors R_X and R_Y must be chosen large enough that non-linear base-emitter voltage variation can be ignored.

C. Care must also be taken to avoid aging and temperature drift in the external components used with the multiplier. This is especially important in the level translation circuitry of Figures 9 and 10.

CHOICE OF CIRCUIT CONSTANTS

Typical element values and power supplies required to provide multiplier operation for two input and output ranges are shown in Table I. In this table, note that the value given for R_3 is approximate; it should be adjusted to set the I_3 which provides the exact gain (K-factor) desired. In some cases, it may be desirable to provide separate power supply regulation for I_3, since the multiplier gain is directly dependent on this current.

LINEARITY

Linearity is measured for V_X and V_Y separately using an x-y plotter with the circuit in Figure 5. It is defined to be the maximum deviation of output voltage from a straight line transfer function expressed as error in percent of full scale, see Figure 11. For example, if the maximum deviation, $V_{E(max)}$, is 100 mV and the full scale output is 10 V, then the error is

$$E_R = \frac{V_{E(max)}}{V_{o(max)}} \times 100$$

$$= \frac{100 \times 10^{-3}}{10\ V} \times 100$$

$$= 1\%$$

To measure this the x-y plotter is set up first to plot V_{out} versus V_X in all four quadrants ($V_Y = \pm 10$ V, $-10\ V \leq V_X \leq +10$ V) then V_{out} versus V_Y ($V_X = \pm 10$ V, $-10\ V \leq V_Y \leq +10$ V). The maximum deviations for x and for y are then determined as shown in Figure 11. It is desirable, but not necessary to zero out the multiplier static error before making this test.

SQUARING MODE ACCURACY

Squaring Mode Accuracy is defined as the maximum absolute deviation from a square law curve expressed as a percent of full scale output. This deviation may be measured by connecting the x and y inputs together (squaring mode) and plotting output versus input, $-10\ V \leq V_X = V_Y \leq +10$ V, using an x - y plotter. Before carrying out this test, the multiplier static error must be zeroed out.

POWER DISSIPATION

Because this circuit has no direct positive power supply connections, power dissipation, P_D, within the actual IC package should be calculated as the summation of the voltage-current products at each port (neglect base currents).

Under normal operating conditions, (Ref. to Figure 5), it is valid to assume:

$$I_2 = I_{14} = I_{13},\ I_1 = 2I_3, \text{ and } V_2 = V_{14} \qquad (40)$$

then

$$P_D = 2\,(V_2 - V_7)\,I_{13} + 2\,(V_1 - V_7)\,I_3 + (V_{13} - V_7)\,I_{13} + (V_3 - V_7)\,I_3 \qquad (41)$$

for the circuit in Figure 11, this is

$$P_D \approx 2\,(36)\,(10^{-3}) + 2\,(29)\,(10^{-3}) + (1.2)\,(10^{-3}) + (1.2)\,(10^{-3})$$

$$\approx 133\ \text{mW}. \qquad (42)$$

BANDWIDTH AND PHASE

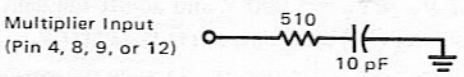
Bandwidth is primarily determined by the load resistors and the stray multiplier output capacitance and/or the operational amplifier used to level shift the output. If wideband operation is desired, small valued load resistors and/or a wideband op amp should be used.

Phase shift in the multiplier circuit results from two sources; phase shift common to both x and y channels (due to the pole at the multiplier output mentioned above), and relative phase shift between x and y channels (due to differences in transadmittance in the x and y channels). If the relative phase shift between channels is only two degrees, the output product of two sine waves will exhibit a maximum magnitude error of 3.5%, which is illustrated in Figure 12. A 2% error due to phase shift occurs at about 200 kHz in the MC1595, and a 3° phase error bandwidth is specified typically as 750 kHz.

PARASITIC OSCILLATION

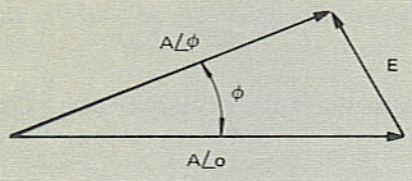
When long leads are used on the input, oscillation may occur. In this event, an R-C parasitic suppression network similar to the one shown below should be connected directly to each input using short leads. The purpose of the network is to reduce the Q of source-tuned circuits which cause the oscillation.

Another technique which is also adequate in most applications is to insert a 510 Ω resistor in series with the multiplier inputs, pins 4, 8, 9, and 12.



APPLICATIONS

The applications of a four-quadrant linear multiplier are almost limitless. Any control or instrumentation prob-



For ϕ small, $E \approx A \sin\phi \approx A\phi$

For $\phi = 2^o$, $\frac{E}{A} \approx 0.0349$

Hence the magnitude of the error vector for 2^o phase error is 3.49% relative.

FIGURE 12 – Relative Phase Error

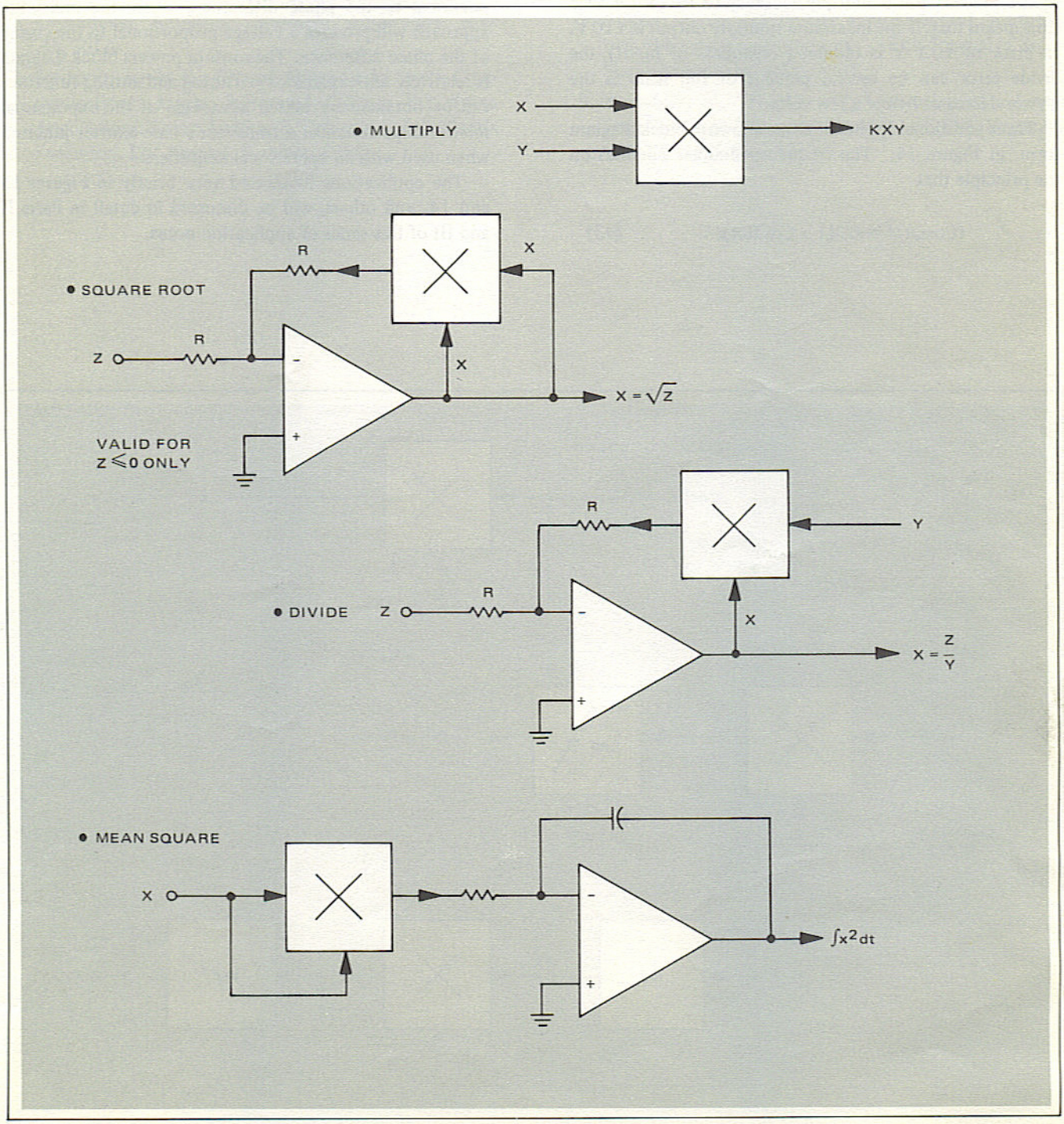


FIGURE 13 – Basic Multiplier Applications

lem requiring the product of two or more quantities is a potential application for the device. The following represents some of the more basic uses of the four-quadrant multiplier, from which more specific applications can be derived. Figure 13 illustrates four basic uses – that of multiplication, division, taking the square root, and obtaining the mean square. In the divide and square root applications, the multiplier is used as a feedback element around an operational amplifier in such a way that the multiplier output is forced to equal the magnitude of the -Z input. The circuit accuracy is somewhat worse in the divide and square root modes than in the multiply or square modes. For a multiply accuracy of 1% of full scale (this means that, if the maximum multiply output is ±10 V, an error of ±0.1 V is obtained regardless of input), the divide error can be several percent of full scale as the divisor decreases below a few volts.

Three additional applications are shown in block diagram form, in Figure 14. The frequency doubler operates on the principle that

$$(\text{Cos}\omega t)^2 = 1/2(1 + \text{Cos}2\omega t), \qquad (43)$$

which results in a dc offset and the doubled frequency signal. The linear phase detector operates on the principle that

$$K\text{Cos}\omega t\text{Cos}(\omega t+\phi)=\frac{K}{2}\text{Cos}(2\omega t+\phi)+\frac{K}{2}\text{Cos}\phi \qquad (44)$$

and with the insertion of a low-pass filter (LPF), the output $\text{Cos}\phi$ is easily obtained. This differs from flip-flop phase detectors or sample-hold phase detectors in that these conventional phase detectors produce a voltage proportional to the phase difference, where the multiplier approach will produce a voltage proportional to the cosine of the phase difference. The roots or powers block diagram is relatively self-explanatory. The log and antilog functions can be obtained by taking advantage of the exponential relationships found in a transistor's base-emitter junction when used with an operational amplifiers.[2]

The applications illustrated very briefly in Figures 13 and 14, and others, will be discussed in detail in Parts II and III of this series of application notes.

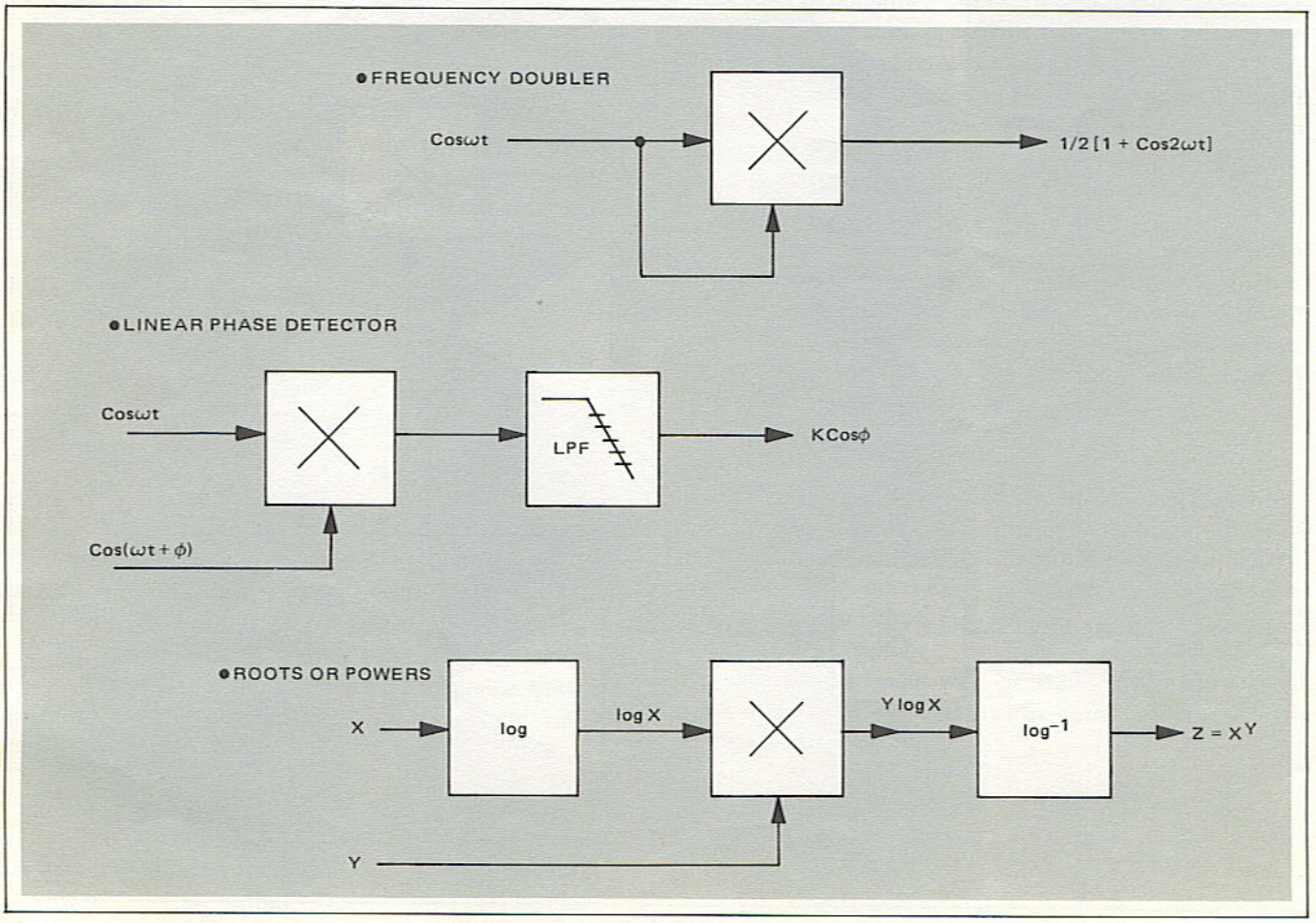


FIGURE 14 – More Basic Applications

ACKNOWLEDGMENT

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REFERENCES

1. EEE Special Survey: Packaged Analog Multipliers, EEE, November, 1968, pp. 80-94.
2. Transistor Logarithmic Conversion Using An Integrated Operational Amplifier, Motorola Application Note AN-261A.
3. Solomon, James E., Recent Advances in Space Communications, Linear Integrated Circuits For Space Applications Series, Lecture 8, University of California Extension, Los Angeles, Summer, 1968.
4. Renschler, E. L., "A New Basic Building Block – The Linear Four-Quadrant Multiplier", Proceedings of the EEE Linear IC Clinic, New York City, March 24, 1969.
5. Renschler, E. L., "New Linear IC Building Blocks for Communications Applications", Proceedings of the 1969 EDN Seminar Series on Applications of Linear IC's, Los Angeles, February 11, 1969, Boston, March 4, 1969, and New York City, March 5, 1969.
6. Free, Maurice G., An Integrated Linear – Transconductance Analog Multiplier, a thesis for the degree of Master of Science in Electrical Engineering at the University of Arizona, Tucson, Arizona, 1969.
7. Gilbert, Barrie, "A Precise Four-Quadrant Multiplier with Subnanosecond Response", IEEE Journal of Solid-State Circuits, December 1968.
8. Renschler, E., "Theory and Application of a Linear Four-Quadrant Monolithic Multiplier", EEE Magazine, Vol. 17, No. 5, May 1969.