

## **Method for a multifrequency clock failure detection circuit**

Disclosed is a method for a multifrequency clock failure detection circuit. Benefits include improved functionality, improved performance, improved reliability, improved power performance, and an improved test environment

### **Background**

Conventionally, modern communication and computer systems rely on clocks for accurate timing. An on-chip clock failure detection circuit enables real-time monitoring of oscillator functionality. When the oscillator malfunctions or is falsely turned OFF, it triggers the detection circuit and signals the microcontroller to respond accordingly. For systems with tunable or programmable oscillators, the detection circuit must tune its frequency detection range (see Figure 1).

Clock failure detection circuits are conventionally based on monostable multivibrators, which fundamentally rely on the real-time clock (RC) time constant to measure the timing.

Requirements for the detection circuit include small size and low power consumption so that the circuit can be deployed on a chip with minimal overhead.

### **General description**

The disclosed method is a multifrequency clock failure detection circuit. The method provides a simple configuration with a low device count and a small size. Power consumption is very low. The circuit is tunable to accommodate a wide frequency range for failure detection and/or compensate for process variations.

The clock failure detection circuit is for use in a laser controller circuit to perform real-time monitoring of the circuit functionality. Alternatively, the clock failure detection circuit provides failure indication for die testing.

### **Advantages**

The disclosed method provides advantages, including:

- Improved functionality due to providing a multifrequency clock failure detection circuit
- Improved functionality due to reducing the circuit size
- Improved performance due to accommodating a wide range of oscillation frequencies
- Improved performance due to compensating for process variation
- Improved reliability due to minimizing the number of components
- Improved power performance due to providing a low-power circuit
- Improved test environment due to providing failure indication for die testing

## Detailed description

The disclosed method is a multifrequency clock failure detection circuit. For example, the incoming clock signal (Clk) is passed into  $\text{Inv}_1$ , which inverts the signal polarity and functions as an input buffer that prevents the diode from loading the previous stage. The realization of  $\text{Inv}_1$  can be a complementary metal oxide semiconductor (CMOS) inverter, a differential pair with active-mirror load, or other topologies, depending on the clock logic. The buffered clock signal is alternating current (AC) coupled, using the  $C_{\text{couple}}$ , to the positive metal oxide semiconductor (PMOS) gate. When no clock is input, the voltage at PMOS gate ( $V_g$ ) is biased at voltage drain ( $V_{dd}$ ) by  $R_{\text{Bias}}$ , and the PMOS is turned OFF. When the clock resumes, each rising edge of Clk causes a down spike at the PMOS gate to turn it ON, enabling a short path to charge capacitor  $C$  to  $V_{dd}$ . Each falling edge of Clk causes an up spike at the PMOS gate, and the highest voltage level is limited by a diode to protect the PMOS from break-down (see Figure 2).

Several resistors ( $R$ ,  $2R$ ,  $4R$ ) are connected in parallel with  $C$  to slowly discharge it. Each resistor is in series with a negative metal oxide semiconductor (NMOS) switch. The total equivalent resistance,  $R_{\text{total}}$ , in parallel with  $C$  can be controlled by signals  $s_2$ ,  $s_1$ , and  $s_0$ . The time constant is selected so that it is slightly longer than the target clock period. The inverter,  $\text{Inv}_2$ , taps the voltage of  $C$  to generate the output signal,  $D_{\text{clk}}$ , to indicate clock malfunction.  $\text{Inv}_2$  can be realized by a CMOS inverter for full-swing output.

When no clock is detected,  $V_g$  keeps its level at  $V_{dd}$ ,  $V_c$  remains at the ground level, and  $D_{\text{clk}}$  is at  $V_{dd}$ . When the first rising edge of the clock arrives, PMOS is turned ON to quickly charge  $V_c$  to  $V_{dd}$ , and  $D_{\text{clk}}$  is pulled down by  $\text{Inv}_2$ . During each clock cycle,  $V_c$  slowly drops at the time constant  $R_{\text{total}} * C$ . The voltage level never falls below the transition point of  $\text{Inv}_2$ , keeping  $D_{\text{clk}}$  low. When the clock signal disappears,  $V_g$  remains at  $V_{dd}$ , PMOS remains off, and  $V_c$  slowly drops to eventually drive  $D_{\text{clk}}$  high (see Figure 3).

The circuit is fully compatible with modern CMOS fabrication technology. Due to the simplicity of the circuit configuration and the small component count, it is highly reliable and small in size if properly designed. It also exhibits capability to manipulate the time constant  $R_{\text{total}} * C$  by controlling  $s_2$ ,  $s_1$ , and  $s_0$  to accommodate a wide range of frequencies. It is possible to achieve a very wide frequency detection range by adding more resistors and associated NMOS switches.

Power consumption of the circuit other than the input buffer is low. In the absence of the incoming clock, power consumption is nominally zero. In the presence of incoming clock, the power consumption is nominally zero at times other than clock transition edges. Currents flow through the PMOS at clock-rising edges. Currents flow through the diode at clock-falling edges. For typical designs, these currents occupy a tiny fraction of a clock period, resulting in a negligible average current consumption.

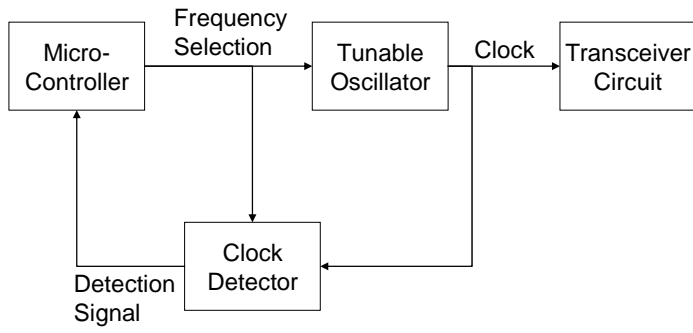


Fig. 1

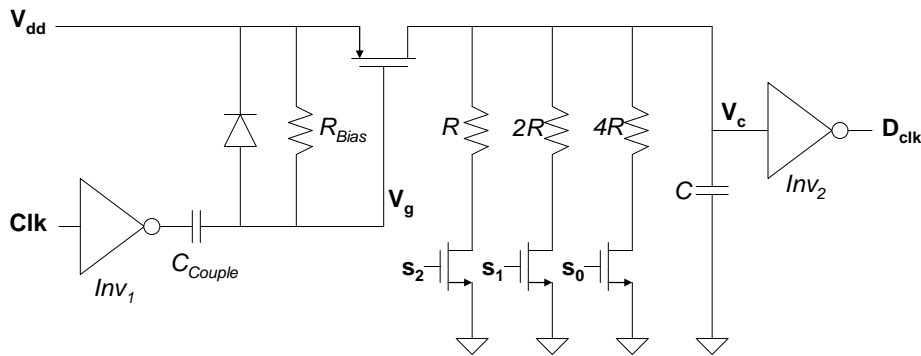


Fig. 2

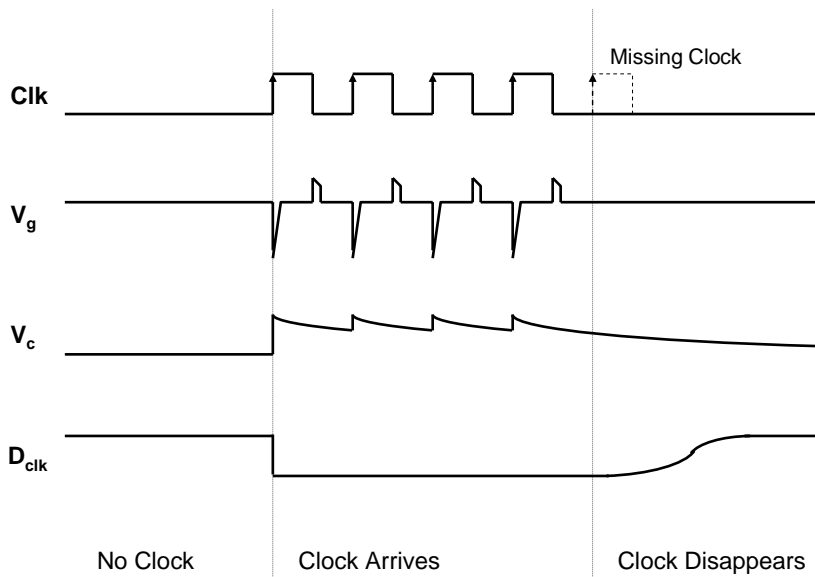


Fig. 3

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